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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/993,387	11/16/2001	Jeffrey Raynor	00ED18852609	4936

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EXAMINER	
DANIELS, ANTHONY J	

ART UNIT	PAPER NUMBER
2622	

DATE MAILED: 06/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/993,387	RAYNOR ET AL.	
	Examiner	Art Unit	
	Anthony J. Daniels	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11,13-30 and 32-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11,13-30 and 32-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 1/25/2006 has been entered.

Response to Arguments

2. Applicant's arguments with respect to claims 11, 21 and 30 have been considered but are moot in view of the new ground(s) of rejection. *The examiner has relied on the same reference, but a new interpretation of the claim is being taken.*

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 11,13-19,21-28,30,32-39 stand rejected under 35 U.S.C. 102(e) as being anticipated by Lee et al. (US # 6,466,265).

As to claim **11**, Lee et al. teaches a solid state imaging device (Figure 2a) comprising: a two-dimensional array of pixels defining an image plane (Figure 2a, pixels "1" – "4"; *{Note the change in the interpretation of the array of pixels. Although the array is formed in a single row, it is a two-dimensional array. Anything that can be seen is two-dimensional.}*); and readout electronics (Figure 2a, channels 1-4-column-address/signal-processing/output "11" – "14") comprising least one store circuit (Figure 5, capacitors "Cr" and "Cs" of the processing circuits "11" and "13"; Col. 5, Lines 36-46) laterally adjacent the image plane for reading signals therefrom (Figure 2a); and a multiconductor signal bus (Figure 2a, wires connected from the pixels "1" - "4" to the processing circuits "11" – "14"; *{Examiner interprets multiconductor signal bus as seen in Figure 6 of the specification; a plurality of wires that connect respective pixels to the readout electronics.}*) connected between said array of pixels and said readout electronics (Figure 2a), said multiconductor signal bus comprising a respective conductor to provide a dedicated readout channel for each and every pixel of said two-dimensional array of pixels defining the image plane (Figure 2a, wires connected between each and all of the pixels "1-4" which as set forth above defines the image plane).

As to claim **13**, Lee et al. teaches a solid state imaging device according to claim 11, wherein each pixel (Figure 2a, pixels "1" – "4") comprises: a photosensitive diode (*A photosensitive diode is inherent in the CMOS pixel array of Figure 2a.*); and a switching circuit for resetting and discharging said diode (Figure 5, Cr (reset value); *{The CDS circuitry of the processing circuits "11" – "14" requires the reset signal of the pixel.}*), said switching circuit consisting of a first transistor for applying a reset pulse, and second transistor for connecting said

diode to a conductor (Col. 1, Lines 59-61, "...active pixel sensors...") within said multiconductor signal bus (Figure 2a).

As to claim **14**, Lee et al. teaches a solid state imaging device according to Claim 11, wherein said multiconductor signal bus comprises plurality of vertically stacked conductors (Figure 2a, wires from pixels "3", "4"; *{Examiner interprets stacked conductors as conductors that are located next to each other as seen in Figure 6 of the specification.}*).

As to claim **15**, Lee et al. teaches a solid state-imaging device according to Claim 11, wherein said readout electronics are laterally adjacent one side of the image plane (Figure 2a, processing circuits "13", "14" to the bottom of the pixel array "10").

As to claim **16**, Lee et al. teaches a solid state imaging device according to Claim 11, wherein said readout electronics are laterally adjacent two opposing sides the image plane (Figure 2a, processing circuits "11", "12" at the top of the pixel array "10"; processing circuits "13", "14" to the bottom of the pixel array '10").

As to claim **17**, Lee et al. teaches a solid state-imaging device according to Claim 11, wherein all pixels of said array of pixels are reset simultaneously and are read out simultaneously (Col. 1, Lines 59-67, Col. 2, Lines 1-8).

As to claim **18**, Lee et al. teaches a solid state imaging device according to Claim 11, wherein said at least one store circuit comprises plurality of store circuits (Figure 2a, Figure 5, capacitors "Cr" and "Cs" of processing circuit "11") with a store circuit corresponding to each pixel (Figure 2a, *{The processing circuit "11" belonging to the pixel "1"*) and comprising: a first store circuit for storing a first reset value (Figure 5, capacitor "Cr"; Col. 5, Lines 36-43); and a second store circuit for storing a read out value (Figure 5, capacitor "Cs"; Col. 5, Lines 36-43),

with the read out value of a given pixel being modified by the stored reset value that pixel (Col. 5, Lines 43-46; *{The difference amplifier "93" of Figure 5 subtracts the reset value from the signal value.}*).

As to claim **19**, Lee et al. teaches a solid state imaging device according to Claim 18, wherein each store circuit further comprises: a third store circuit for storing a second reset value (Figure 2a, Figure 5, capacitor "Cr" of processing circuit "13" from pixel "3"), with a current reset value (Figure 2a, Figure 5, reset value on capacitor "Cr" of processing circuit "11") and a current read out value (Figure 2a, Figure 5, signal value on capacitor "Cs" of processing circuit "11") being processed simultaneously based upon application a new reset pulse (Col. 1, Lines 59-67; Col. 2, Lines 1-8).

As to claims **30,34-39**, claims 30,34-39 are method claims corresponding to the apparatus claims 11,14-19, respectively. Therefore, claims 30,34-39 are analyzed and rejected as previously discussed with respect to the apparatus claims 11,14-19, respectively.

As to claim **21**, Lee et al. teaches a solid state imaging device (Figure 2a) comprising: a two-dimensional array of pixels defining an image plane (Figure 2a, pixels "1" – "4"; *{Note the change in the interpretation of the array of pixels. Although the array is formed in a single row, it is a two-dimensional array. Anything that can be seen is two-dimensional.}*), each pixel comprising a photosensitive diode (*A photosensitive diode is inherent in the CMOS pixel array of Figure 2a.*), switching circuit for resetting and discharging said diode (Figure 5, Cr (reset value); *{The CDS circuitry of the processing circuits "11" – "14" requires the reset signal of the pixel.}*); a multiconductor signal bus connected to said array pixels (Figure 2a, wires connected from the pixels "1" - "4" to the processing circuits "11" – "14"; *{Examiner interprets signal bus*

as seen in Figure 6 of the specification; a plurality of wires that connect respective pixels to the readout electronics.}), said multiconductor signal bus comprising a respective conductor to provide a dedicated readout channel for each and every pixel of said two-dimensional array of pixels defining the image plane (Figure 2a, wires connected between pixels "1-4"); and readout electronics (Figure 2a, channels 1-4-column-address/signal-processing/output "11" – "14") comprising at least one store circuit (Figure 5, capacitors "Cr" and "Cs" of the processing circuits "11" and "13"; Col. 5, Lines 36-46) laterally adjacent the image plane and connected to the multiconductor signal bus for reading signals from said array of pixels (Figure 2a, wires connected between each and all of the pixels "1-4" which as set forth above defines the image plane).

As to claim **22**, Lee et al. teaches a solid state imaging device according to Claim 21, wherein said signal bus comprises a multiconductor signal bus (Figure 2a, wires connected from the pixels "1" - "4" to the processing circuits "11" – "14"; *{Examiner interprets multiconductor signal bus as seen in Figure 6 of the specification; a plurality of wires that connect respective pixels to the readout electronics.}*); and wherein said switching circuit consisting of a first transistor for applying a reset pulse, and second transistor for connecting said diode to a conductor (Col. 1, Lines 59-61, "...active pixel sensors...") within said multiconductor signal bus (Figure 2a).

As to claim **23-28**, the limitations in claims 23-28 can be found in claims 14-19, respectively. Therefore, claims 23-28 are analyzed and rejected as previously discussed with respect to claims 14-19, respectively.

As to claim **32**, Lee et al. teaches a method according to Claim 30, further comprising forming each pixel to have a photosensitive diode (*A photosensitive diode is inherent in the CMOS pixel array of Figure 2a.*), and a switching circuit connected thereto for resetting and discharging the diode (Figure 5, Cr (reset value); *{The CDS circuitry of the processing circuits "11" – "14" requires the reset signal of the pixel.}*).

As to claim **33**, Lee et al. teaches a method according to Claim 32, wherein the switching circuit consists essentially of a first transistor for applying a reset pulse, and second transistor for connecting said diode to a conductor (Col. 1, Lines 59-61, "...active pixel sensors...") within said multiconductor signal bus (Figure 2a).

Claim Rejections - 35 USC § 103

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 20,29,40 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (see Patent Number above) in view of Decker et al. (US 20020154231).

As to claim **20**, Lee et al. teaches a solid state imaging device according to Claim 19, wherein said readout electronics further comprises: a differential amplifier (Figure 5, difference amplifier "93") connected to said first, second and third store circuits (Figure 2a, Figure 2e, Figure 5). The claim differs from Lee et al. in that it further requires a reset circuit for placing said differential amplifier a common mode reset state prior to reading a signal.

In the same field of endeavor, Decker et al. teaches a CMOS imaging array (Figure 3) with readout electronics including a CDS circuit including a difference amplifier (Figure 7, amp "700") that is put into a common-mode state upon receiving a pulse signal at a transistor (Figure 7, transistor "M705"; $\phi 1$; [0065], Lines 7-15). In light of the teaching of Decker et al., it would have been obvious to one of ordinary skill in the art to include the ability of the difference amplifier of Lee et al. to be put in a common-mode state thereby ensuring the correct difference between the signal values and reset values.

As to claim **29**, the limitations of claim 29 can be found in claim 20. Therefore, claim 29 is analyzed and rejected as previously discussed with respect to claim 20.

As to claim **40**, claim 40 is a method claim corresponding to the apparatus claim 20. Therefore, claim 40 is analyzed and rejected as previously discussed with respect to claim 20.

Conclusion

5. *The examiner would like to submit that section II of the Remarks ("The Claims are Patentable") has been thoroughly considered. The examiner would also like to make a suggestion in regard to the claimed invention and the Lee et al. reference. First, the present invention, if the examiner understands it correctly, provides a multiconductor signal bus comprising a respective conductor providing a dedicated readout channel for each and every pixel of a solid-state imaging device. Furthermore, each said respective conductor provides a dedicated readout channel for* ***only one pixel****. The Lee et al. reference also teaches a multiconductor signal bus comprising a respective conductor providing a dedicated readout channel for each and every pixel of a solid-state imaging device. However, the Lee et al. reference provides a dedicated readout channel* ***to multiple pixels****, due to the multiplexing nature of the invention. Examiner believes that an amendment of this sort to the claims would be a good step in amending over the Lee et al. reference.*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony J. Daniels whose telephone number is (571) 272-7362. The examiner can normally be reached on 8:00 A.M. - 5:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ngoc-Yen Vu can be reached on (571) 272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AD
5/24/2006

TUAN HO
PRIMARY EXAMINER